MW_DVBS2 Modulator Core

BROADCASTING

General Description

The MW_DVBS2 modulator core performs the digital baseband functionality for the transmission side of Digital Video Broadcasting Satellite link.
The modulator core implements the framing functions as defined by ETSI EN 302 307 V1.1.1 (2009-08).
It is configurable to supports all configurations regard to constellation 4QAM, 8PSK, 16 APSK and 32APSK, code rate 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 5/6, 8/9 and 9/10.
The error protection used is based on LDPC algorithm followed by the bit interleaver.
Squared-root raised cosine filter, with roll-off factors 0,35 or 0,25 or 0,20 is used.
Microblaze or external processor interface, with status and control registers, is available for controlling and managing the core.
TS over IP is available, for IP based contribution. ASI interface is available too.
Internal 20-bit architecture for high level MER and BER performances.
FPGA netlist only or complete design environment package are deliverable.

Features

- Compliant with ETSI EN 302 307 V1.2.1 (2009-08)
- Support all code rate, all constellation type
- Support Single and Multiple stream
- Internal or external microcontroller interface
- AD9747 or AD9789 interface available, with interpolation stages. Other DAC interfaces are available under customer request
- Typical MER > 43 dB at UHF band
- SRRC filter used
- Digital Linear – Non Linear – Group Delay Precorrection Option

Performance and Resources Utilization

Family	Device	Slices	SliceReg	LUTs	DSP 48E1	Bram	Speed (MHz)
Artix 7	XC7A200T	3521	8942	8894	14	49	160

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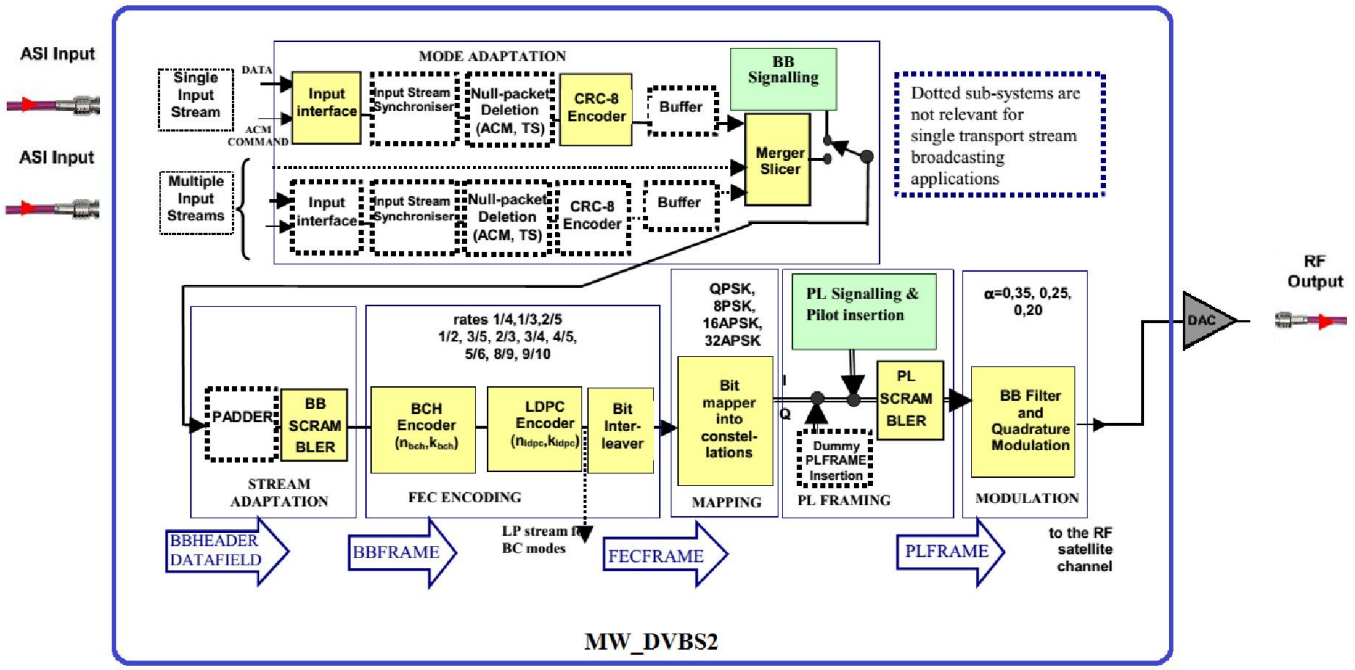
Typical Application



Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:
http://www.mindway-design.com

or send an e-mail at:

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