BROADCASTING

MW_DVBTH_7S Modulator Core

General Description

The MW_DVBTH_7S modulator core performs the digital baseband functionality for the transmission side of Digital Video Broadcasting Terrestrial link.
The modulator core implements the framing functions as defined by ETSI EN 300 744 V1.5.1 (2004-11).
The modulator core is deliverable in DVB-T and DVB-H functionality, ASI based contribution.
It is configurable to supports all several configurations regard to constellation, 4QAM, 16QAM and 64QAM, code rate, 1/2, 2/3, 3/4, 5/6 and 7/8, guard interval, 1/32, 1/16, 1/8 and 1/4, 2K-4K-8K.
A reduced 2k compact version of the DVB-T/H core is deliverable.
Microblaze or external processor interface, with status and control registers, is available for controlling and managing the core.
External memories (SDRAM and DDR) are used to support SFN functionality. A dedicated interface is perfomed.
TS over IP is available, for IP based contribution.
A direct interfave with Analog Devices AD9789, covering VHF-UHF bands is available.
Internal 20-bit architecture for high level MER and BER performances.
FPGA netlist only or complete design environment package are deliverable.

Features

- Fully compliant with ETSI EN 300 744 V1.5.1 (2004-11)
- Support DVB-H functionality
- Configurable for 2k, 4k and 8k OFDM modes
- Support all code rate, all constellation type and all guard interval
- Support Hierarchical-Non Hierarchical Mode
- Internal or external microcontroller interface
- External SDRAM - DDR2 memory interface
- AD9747 interface available, with interpolation stages
- Typical MER > 43 dB at overall frequency range
- Single Frequency Network Option
- Digital Linear – Non Linear – Group Delay Precorrection Option

Performance and Resources Utilization

Family	Device	Slices	SliceReg	LUTs	DSP 48E1	Bram	Speed (MHz)
Artix 7	XC7A200T	4386	16241	13451	103	71	146

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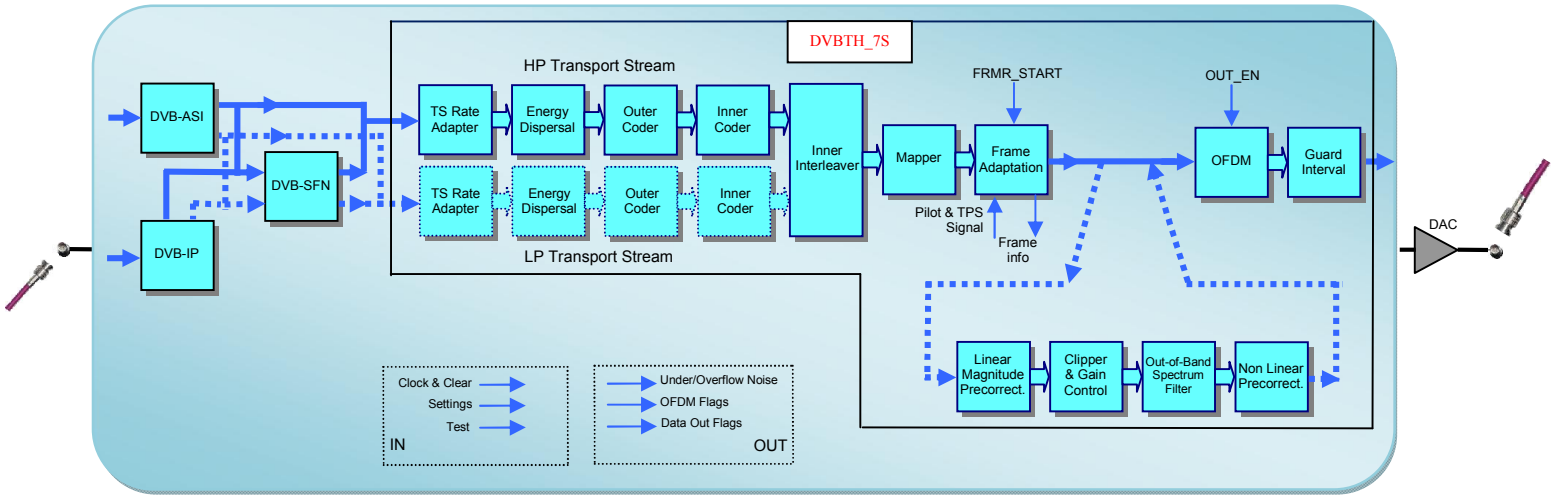
Typical Application



Available configuration

CORE P/N	Functionality
➢ MW_DVB_7S-ASI	DVB Asi SerDes interface
➢ MW_DVB_7S-IP	DVB IP interface
➢ MW_DVB_7S-SFN	DVB SFN Synchronization for hierachical mode working
➢ MW_DVBTH_7S	DVB T/H base modulation
➢ MW_DVBTH_7S_A	MPEG-2 TS (Transport Stream) adaptation
➢ MW_DVBTH_7S_P	DVB T/H base modulation with added linear magnitude precorrection
➢ MW_DVBTH_7S_F	DVB T/H Gain Control and Out-of-Band Spectrum Filtering (ETSI EN 300 744 v1.5.1 2006-11, par. 4.8.2)
➢ MW_DVBTH_7S_PF	DVB T/H Linear/Non-Linear predistorsion, Gain Control and Out-of-Band Spectrum Filtering (ETSI EN 300 744 v1.5.1 2006-11, par. 4.8.2)

Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:
http://www.mindway-design.com

or send an e-mail at:

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