MW_DVB_FEC Core

General Description

The MW_DVB_FEC core performs the digital baseband function Forward Error Correction (FEC) for the transmission side of new generation Digital Video Broadcasting system.
The FEC core implements the BCH/LDPC functions as defined by ETSI EN 302 755 and by ETSI EN 302 307; t-error correction BCH code shall be applied to each frame to generate an error protected packet; this shall be systematically encoded with LDPC before bit interleaving.
The FEC core supports short and long FEC blocks, 16,200 bits and 64,800 bits, as defined by the standard:

short FECFRAME N_{ldpc} = 16 200

LDPC Code identifier	BCH Uncoded Block K_{bch}	BCH coded block N_{bch} LDPC Uncoded Block K_{ldpc}
1/4 (see note)	3 072	3 240
1/2	7 032	7 200
3/5	9 552	9 720
2/3	10 632	10 800
3/4	11 712	11 880
4/5	12 432	12 600
5/6	13 152	13 320

normal FECFRAME N_{ldpc} = 64 800

LDPC Code	BCH Uncoded Block K_{bch}	BCH coded block N_{bch} LDPC Uncoded Block K_{ldpc}
1/2	32 208	32 400
3/5	38 688	38 880
2/3	43 040	43 200
3/4	48 408	48 600
4/5	51 648	51 840
5/6	53 840	54 000

It support all code rate also for both short and normal frame.
The core is designed to achieve high performance for a single chip FPGA based design, including control and status management.
The core was developed in Vivado tool, written in HDL code.

Rate, frame size can be changed frame by frame independently.
Structural simulation and hardware test was performed to check compliant with DVB-T2 Verification & Validation Working Group reference, used their reference stream input and to compare encoded FEC frame after LDPC.
FPGA netlist only or complete design environment package are deliverable.

Features

- Compliant with ETSI EN 302 755 V1.3.1 2011-11, for DVBT2, and ETSI EN 302 307 V1.2.1 2009-08
- FEC length : short 16,200 bits, and long 64,800 bits
- Code Rate : 1/4, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6
- Synchronous design using single clock
- Low complexity design
- Independently configuration frame by frame
- Very fast FEC block encoded output, 16,223 clock cycles for short frame and 64,823 clock cycles for normal frame
- Very high troughput, near real time
- Small resource utilization :

Slices	Slice Reg	LUTs	LUTRAM	BRAM/FIFO	DSP48E1
910	1910	2860	49	19	0

- Zynq/Artix7 technology and ISE Xilinx 14.7/ Vivado tool

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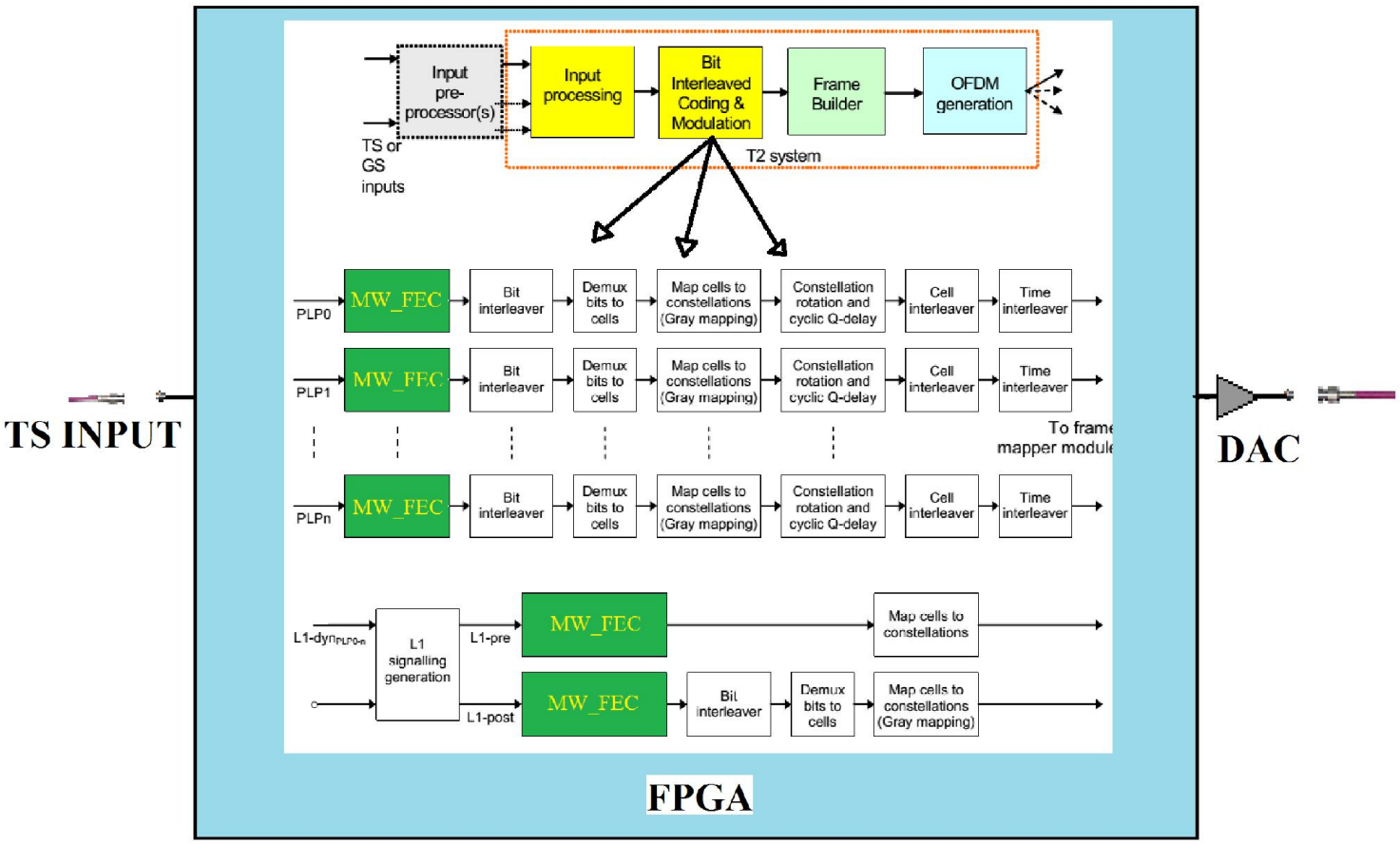
Typical Application



Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:

http://www.mindway-design.com

or send an e-mail at:

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