MW_FSIM Modulator Core

General Description

The MW_FSIM modulator core performs the physical layer for Return Link Asynchronous Access of the transmission side of a Satellite system.

F-SIM asynchronous access is intended for access to interactive messaging services, with a single transport channel called Random Access Channel (RACH), and two physical channel called Physical Data Channel (PDCH) and Physical Control Channel (PCCH). PDCH is used to carry the RACH data burst, and the PCCH is used to carry physical layer signalling information; both channels are I/Q code multiplexed to form an Up-Link Burst (ULB), with a preamble followed by PDCH/PCCH.

Six different possible sizes of the RACH data burst length are supported (in total bits), namely 960, 1920, 3600, 7200, 14400 and 36000 bits, and three allowed symbols rate are present, called chip rate, 1920, 3840 and 7680 kchip/s. Depending on the effective size of the RACH data burst length and of the size of the CRC, rate matching will be performed after FEC encoding (Turbo-coder 1/3).

To be remarked that to cope with the FEC interleaving size limitation of 5114 bits, large burst lengths are obtained concatenating consecutive FEC frames.

After interleaving and mapping, a channelization operation, with OVSF code, transforms every symbol into a number of chips, and then a scrambling code is used to spread signal, the same scrambling solution as foreseen in 3GPP WCDMA.

F-SIM modulator core was developed in Vivado tool, written in HDL code, and tested on Xilinx Artix™ 7 series and Xilinx Zynq™ FPGA.

Rate, frame size, OVSF code, scrambling and other parameters can be changed frame by frame independently.

Structural simulation and hardware test was performed to check compliant with Matlab model.
Return Link Encapsulation core can be included also.
FPGA netlist only or complete design environment package are deliverable.

Features

- Fully compliant with F-SIM Physical Layer Specification, developed by Eutelsat

- Six data burst length of RACH channel: 960, 1920, 3600, 7200, 14400 and 36000 bits

- Channel bandwidth : 10, 5, 2.5 MHz

- FEC encoding with Turbo-coder 1/3

- OVSF code for channelization

- 3GPP WCDMA scrambling solution

- Frequency and time (chip, bit, burst) synchronization

- Low complexity design

- Independently configuration frame by frame

- Resource utilization:

Slices	Slice Reg	LUTs	LUTRAM	BRAM/FIFO	DSP48E1
7914	16351	16798	4446	95	88

- Zynq/Artix7 technology and ISE Xilinx 14.7/ Vivado tool
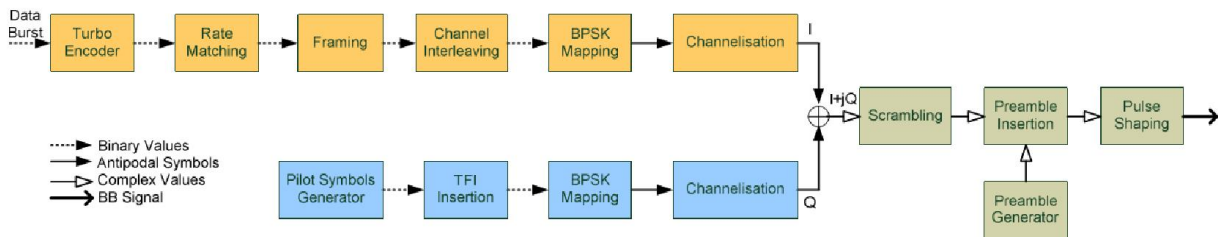
Typical Application
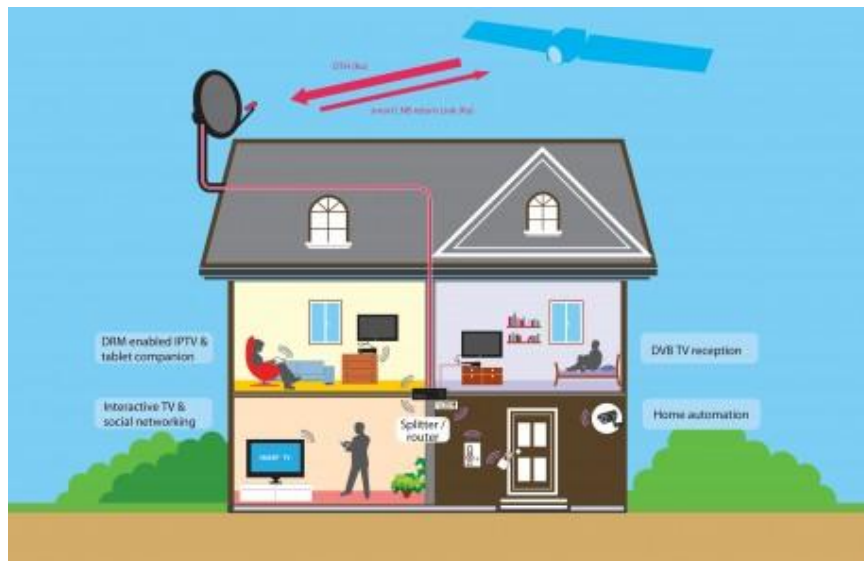
Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:

http://www.mindway-design.com

or send an e-mail at:

info@mindway-design.com