BROADCASTING

MW_ISDBT/Tb Modulator Core

General Description

The MW_ISDBT/Tb modulator core performs the digital baseband functionality for the transmission side of Japanese-Brazilian Integrated Services Digital Broadcasting Terrestrial link.
The modulator core implements the framing functions as defined by ARIB STD B31 (2005-11).
It is configurable to supports all several configurations regard to constellation, DQPSK, 4QAM, 16QAM and 64QAM, code rate, 1/2, 2/3, 3/4, 5/6 and 7/8, guard interval, 1/32, 1/16, 1/8 and 1/4, 1k-2k-4k-8k.
Microblaze or external processor interface, with status and control registers, is available for controlling and managing the core.
External memories (SDRAM and DDR) are used to support SFN functionality.
TS over IP, for IP based contribution, or ASI contribution are available.
A direct interface with Analog Devices AD9789, covering VHF-UHF bands is implemented.
Internal 20-bit architecture for high level MER and BER performances.
FPGA netlist only or complete design environment package are deliverable.

Features

- Compliant with ARIB STD B31 (2005-11)
- Fully Synchronous design
- Mode 1-2-3 supported
- Support all code rate, all constellation type and all guard interval
- Support Hierarchical Layers
- MFN and SFN functionalities
- Internal or external microcontroller interface
- Support TMCC & AC1/AC2 channel input ports for dynamic operation
- External SDRAM - DDR2 memory interface
- AD9789 direct VHF-UHF conversion interface available
- Typical MER > 43 dB at overall frequency range
- Digital Linear – Non Linear – Group Delay Precorrection Option

Performance and Resources Utilization

Family	Device	Slices	SliceReg	LUTs	DSP 48E1	Bram	Speed (MHz)
Artix 7	XC7A200T	5285	19241	16038	122	85	75

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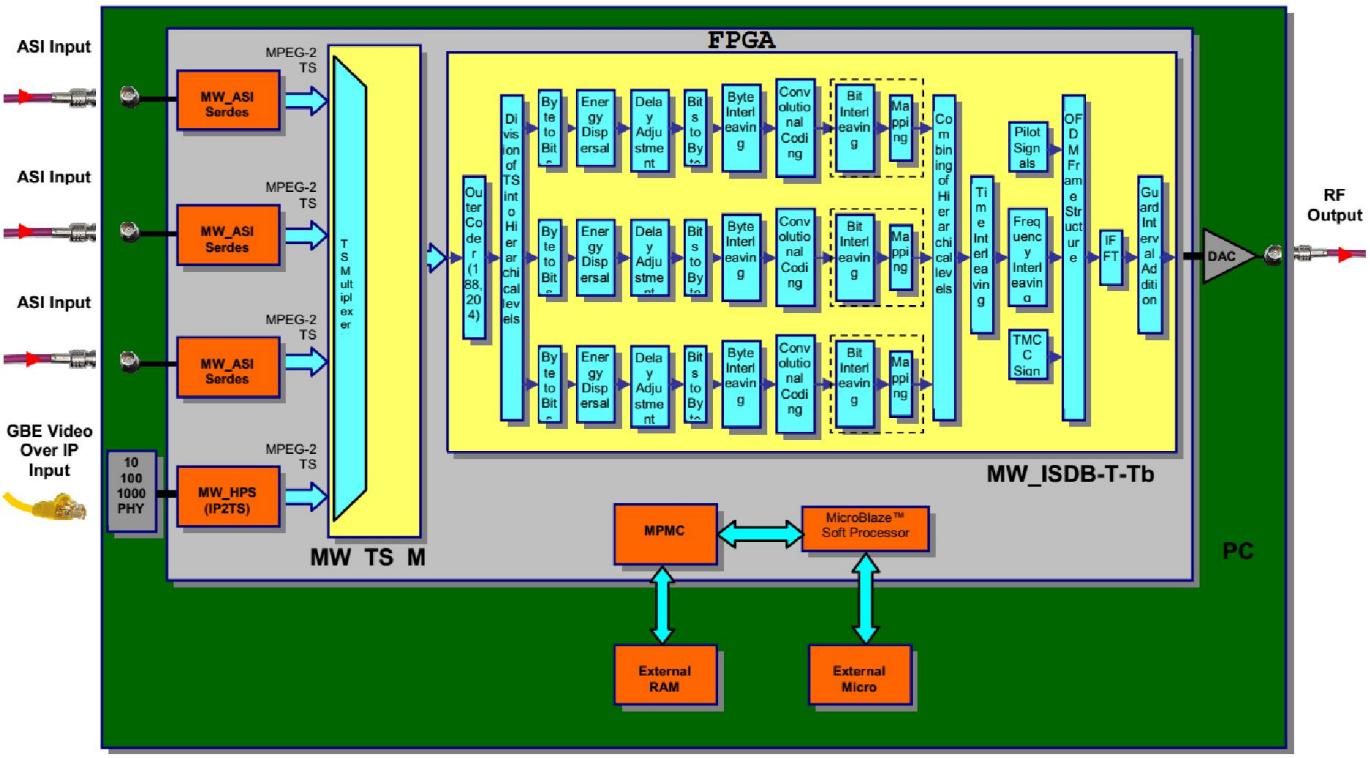
Typical Application



Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA netlist and Xilinx ISE constraint files
- User guide
- Block level design document
- VHDL test bench and test vectors

Optional deliverables:

- Fully synthesizable VHDL source code
- Synthesis script for XST

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:
http://www.mindway-design.com

or send an e-mail at:

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