MW_RR : FPGA Remote Reconfiguration

General Description

The MW_RR, FPGA Remote Reconfiguration, is a set of core, desktop and embedded software applications provided to enable the remote reconfiguration of an FPGA device, booting from an external Flash memory.

Remote configuration is a critical feature for complex electronic systems. In a wide range of applications, the hardware to be reconfigured is not directly accessible by the user, for debugging or upgrading purposes. Furthermore, the introduction of dedicated connections intended to remotely access the device is something difficult and expensive.

Programmable System-on-Chip platforms greatly make Remote Configuration task easier. For instance an OS-based design gives the opportunity to load the new configuration file at many stages of software booting and execution and to use standard interfaces (Ethernet, USB, SD Card, etc.) to transfer such files.

When using traditional FPGAs, usually there are less degrees of freedom to achieve the task, and anyway the procedure is much more complex.

The MW_RR exploits the benefits of standard OS solution to remotely reconfigure an FPGA. The advantage of such a kind of approach is threefold:

1. When performing a batch (re-)configuration, there is no need to have a JTAG daisy-chain for all devices (thus enabling scalability). This is also true for configuration readback and verification.
2. In a system with a processor/SoC driving the FPGA, the procedure is spread between the processor acting as a Master for both read and write operations and the FPGA being a slave.
3. In any case, there is no need of using an additional off-chip JTAG programmer and a proprietary tool to interact with it.

In the case 1 the PC interacts with the device with a set of commands to assert the link consistency (an immediate feedback is provided with the toggle of a pair of LEDs), to set the target sector and page on the configuration memory and to read and write pages. The commands can be batched to cover the overall configuration file or flash extent.

The PC interface is a standard COM port while the target device interface is a simple UART port. The readback output is dumped on ASCII files on the user PC. Each atomic operation is individually acknowledged.

In the case 2 the configuration file is transferred to the master processor by means of an SCP protocol (alternatively, the file can reside on the non-volatile File system). The application is in charge of transmitting the file page by page.

The MW_RR needs an alive embedded processor (for instance a Microblaze) to provide both the interface and the software routine to transfer the configuration files. If such a processor already exists, only the software routine needs to be added to the user application, at the cost of the only additional occupancy of the Flash Memory controller on the device.

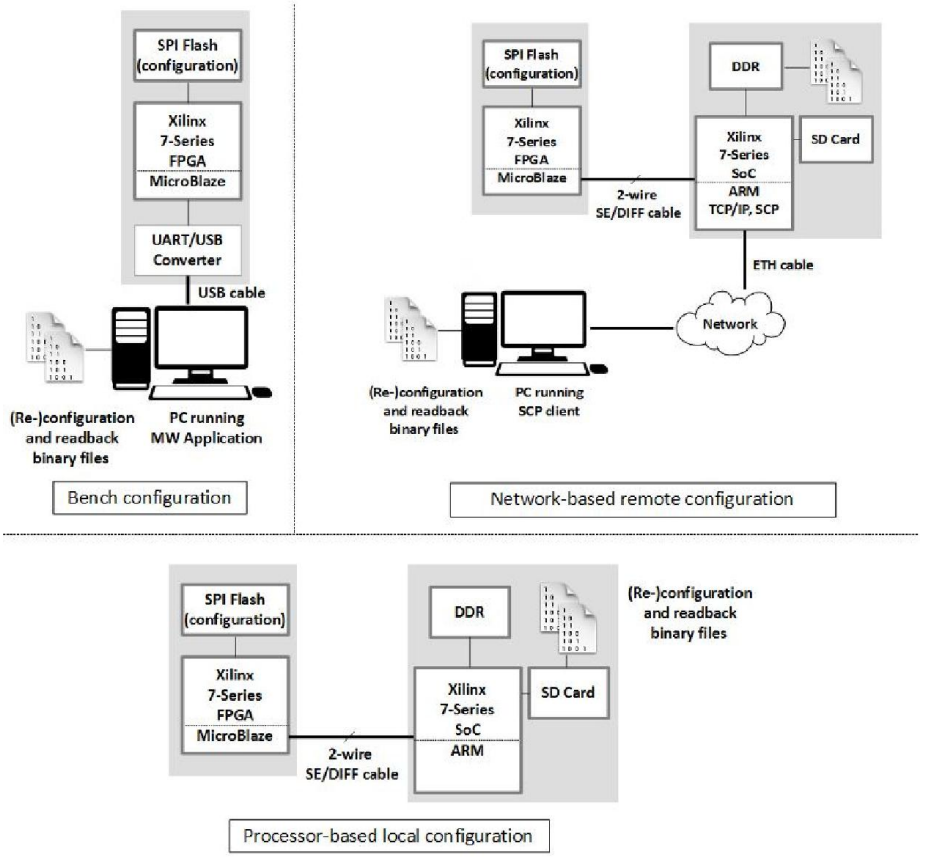
Multiboot is also supported, allowing the FPGA to load two or more FPGA bitstreams. The FGPA triggers a MultiBoot operation, causing the device to reconfigure from a different configuration bitstream. This is particularly important to recover to a golden bitstream in the case of an unsuccessful hardware/software upgrade.

Features

- 2-wire general purpose interface for device access.
- Functionality can be added even if it was not conceived at an early design stage.
- Readback capability.
- Desktop environment support.
- Embedded environment support.
- Network-based (SCP) configuration file transfer.
- Error protection over the duplex master-slave link.
- Multiple boot support.
- Zynq/Artix7 technology and ISE Xilinx /Vivado tool

Family	Device	Slices	SlicesReg	LUTs	DSP 48E1	Bram	Speed (MHz)
Artix 7	XC7A200T	6255	5600	6015	0	30	

Typical Application



Support

The core, delivered as is, is warranted against defects for two years from the date of purchase. Sixty days of phone and email technical support are included, starting from the delivery date.

Verification

The core has been verified through extensive simulation and physical implementation on Xilinx Artix™ 7 and Xilinx Zynq™ FPGA technology.

Deliverables

The following deliverables are available:

- FPGA bit-stream, software application
- User guide
- Block level design document

Optional deliverables:

- Fully synthesizable VHDL source code
- C code
- Synthesis script

Please feel free to require any further information. Other MindWay Core Solutions are available, for standard or custom design applications, please visit our web site:

http://www.mindway-design.com

or send an e-mail at: